Docket No. 239736US2hc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Hiroshi MATSUSHITA

SERIAL NO: 10/608,155 GAU: 2133

FILED: June 30, 2003 EXAMINER:

FOR: FAILURE ANALYSIS SYSTEM, FAILURE ANALYSIS METHOD, A COMPUTER PROGRAM PRODUCT AND A MANUFACTURING METHOD FOR A SEMICONDUCTOR DEVICE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:
Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

■ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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Form PTO 1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 239736US2	SERIAL NO. 10/608,155
LIST OF REFERENCES CITED BY APPLICANT	APPLICANT Hiroshi MATSUSHITA	
	FILING DATE June 30, 2003	GROUP 2133

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO					
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	H. MATSUSHITA, et al., IEEE Transactions on Semiconductor Manufacturing, vol. 15, no. 4, pages 1-7, "HIGHLY SENSITIVE INSPECTION SYSTEM FOR LITHOGRAPHY-RELATED FAULTS IN AGILE-FAB - DETECTING ALGORITHM FOR MONITORING AND EVALUATION OF YIELD IMPACT", November 2002
	AX	K. MITSUTAKE, et al., Proc. 10th Int. Symp. Semiconductor Manufacturing, pages 247-250, "NEW METHOD OF EXTRACTION OF SYSTEMATIC FAILURE COMPONENT", 2001
	AY	M. SUGIMOTO, et al., Proc. 10th Int. Symp. Semiconductor Manufacturing, pages 275-278, "CHARACTERIZATION ALGORITHM OF FAILURE DISTRUBUTION FOR LSI YIELD IMPROVEMENT", 2001
	AZ	K. NAKAMAE, et al., Proc. 4th Int. Conf. Modeling and Simulation of Microsystems, pages 598-601, "FAIL PATTERN CLASSIFICATION AND ANALYSIS SYSTEM OF MEMORY FAIL BIT MAPS", 2001

☐ Additional References sheet(s) attached

Examiner	Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.